WHAT IS CLAIMED IS:

1	1.	A method of forming a memory, the method comprising:	
2		providing a substrate having a non-volatile memory region and a volatile memory	
3	region;		
4		forming bottom electrodes of storage capacitors in the volatile memory region;	
5		forming a first dielectric layer on the substrate;	
6		forming a first polysilicon layer on the first dielectric layer;	
7		forming a poly-oxide layer of a split-gate transistor in the non-volatile memory	
8	region;		
9		etching the first polysilicon layer to form a floating gate of a split-gate transistor;	
10		forming a top electrode of a capacitor; and	
11		forming a control gate of the split-gate transistor.	
1	2.	The method of claim 1 wherein the step of forming bottom electrodes is performed	
2	by:		
3		patterning a mask to expose portions of the substrate where the storage capacitors	
4	are to be located; and		
5		implanting the exposed portions of the substrate.	
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- 1 3. The method of claim 2 wherein the mask includes a pad oxide layer.
- 1 4. The method of claim 2 wherein the mask includes a silicon nitride layer.
- 1 5. The method of claim 1 wherein the step of forming the poly-oxide is performed by:
- 2 forming a second mask on the first polysilicon layer;
- 3 patterning the second mask to expose portions of the first polysilicon layer; and
- 4 oxidizing the exposed portions of the first polysilicon layer.
- 1 6. The method of claim 5 wherein the second mask is a hard mask comprising silicon
- 2 nitride.
- 1 7. The method of claim 6 wherein the step of patterning the second mask includes
- 2 etching the second mask using a dry plasma etch process.
- 1 8. The method of claim 1 wherein the steps of etching the first polysilicon layer to
- 2 form a floating gate and forming the top electrode are performed in the same process step.
- 1 9. The method of claim 1 wherein the steps of forming the control gate and forming
- 2 the top electrode are performed in the same process step.

2	providing a substrate;		
3	forming bottom electrodes of a capacitor;		
4	forming a first dielectric layer on the substrate;		
5	forming a first polysilicon layer on the first dielectric layer;		
6	oxidizing a first portion of the first polysilicon layer to form a first poly-oxide layer		
7	a split-gate transistor;		
8	oxidizing a second portion of the first polysilicon layer to form a second poly-oxide		
9	layer to define a portion of the first polysilicon layer that is to become a top electrode of a		
10	capacitor;		
11	etching the first polysilicon layer to form a floating gate of a split-gate transistor		
12	and a top electrode of a capacitor; and		
13	forming a control gate of the split-gate transistor.		
1	11. The method of claim 10 wherein the capacitor is formed along the edge of a		
•	The method of claim to wherein the capacitor is formed along the cage of a		
2	shallow trench isolation.		
1	12. The method of claim 10 wherein the step of forming bottom electrodes is		
2	performed by:		
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A method of forming a memory, the method comprising:

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4	are to be located; and		
5		implanting the exposed portions of the substrate.	
1	13.	The method of claim 12 wherein the mask includes a pad oxide layer.	
1	14.	The method of claim 12 wherein the mask includes a silicon nitride layer.	
1	15.	The method of claim 10 wherein the step of oxidizing the first portion is performed	
2	by:		
3		forming a second mask on the first polysilicon layer;	
4		patterning the second mask to expose portions of the first polysilicon layer; and	
5		oxidizing the exposed portions of the first polysilicon layer.	
1	16.	The method of claim 15 wherein the second mask is a hard mask comprising silicon	
2	nitride.		
1	17.	The method of claim 16 wherein the step of patterning the second mask includes	
2	etchin	ng the second mask using a dry plasma etch process.	
1	18.	The method of claim 10 wherein the step of oxidizing the second portion is	
2	performed by:		
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patterning a mask to expose portions of the substrate where the storage capacitors

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- forming a third mask on the first polysilicon layer;
- 4 patterning the third mask to expose portions of the first polysilicon layer; and
- 5 oxidizing the exposed portions of the first polysilicon layer.
- 1 19. The method of claim 18 wherein the third mask is a hard mask comprising silicon
- 2 nitride.
- 1 20. The method of claim 19 wherein the step of patterning the third mask includes
- 2 etching the third mask using a dry plasma etch process.
- 1 21. The method of claim 10 wherein the step of forming a floating gate of a split-gate
- 2 transistor and a top electrode of a capacitor is performed in the same process step.

2 a volatile memory region including: 3 a bottom capacitor electrode; 4 a dielectric layer patterned to form a capacitor dielectric; and 5 a polysilicon layer patterned to form a top capacitor electrode; 6 a non-volatile memory region including: 7 said dielectric layer patterned to form a tunneling gate dielectric of a 8 split-gate transistor; 9 said polysilicon layer patterned to form a floating gate of the split gate 10 transistor; and 11 a poly-oxide region formed in said polysilicon layer substantially 12 self-aligned with the floating gate. 1 23. The integrated circuit of claim 22, wherein the bottom capacitor electrode is formed 2 a portion of a substrate that has been doped. 1 24. The integrated circuit of claim 22, wherein the bottom capacitor electrode is formed 2 along the edge of a shallow trench isolation.

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An integrated circuit comprising: